REMARKS

The Final Office Action of October 6, 2006, has been received and reviewed.

Claims 1-14 are currently pending and under consideration in the above-referenced application, each standing rejected.

Reconsideration of the above-referenced application is respectfully requested.

Supplemental Information Disclosure Statement

Please note that a Supplemental Information Disclosure Statement was filed in the above-referenced application on October 3, 2006, but that the undersigned attorney has not yet received any indication that the references cited in the Supplemental Information Disclosure Statement have been considered in the above-referenced application. It is respectfully requested that the reference cited in the Supplemental Information Disclosure Statement of October 3, 2006, be considered and made of record in the above-referenced application and that an initialed copy of the Form PTO/SB/08A that accompanied that Supplemental Information Disclosure Statement be returned to the undersigned attorney as evidence of such consideration.

Rejections under 35 U.S.C. § 103(a)

Claims 1-14 stand rejected under 35 U.S.C. § 103(a).

The standard for establishing and maintaining a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Saka in View of Sahota

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in U.S. Patent 6,476,921 to Saka et al. (hereinafter "Saka"), in view of teachings from U.S. Patent 5,665,199 to Sahota et al. (hereinafter "Sahota").

Saka teaches a system that uses reflectance to analyze a wafer *during polishing* and selectively applies different amounts of pressure to the *same wafer* in response to the analyzed reflectance to improve the planarity of a polished surface of the wafer. *See, e.g.,* Abstract; FIG. 4; col. 7, lines 14-56.

Sahota teaches methods for developing polishing processes that are tailored to specific types of material layers. The methods of Sahota are used to improve planarity of the polished layers. The tailoring techniques disclosed in Sahota are limited to use of conventionally configured polishing pads and substrate supports, in which there is no application of different amounts of pressure to either the pad or the substrate. Rather, it is the duration of the polishing process that is tailored.

It is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 1-14 because, assuming the system of Saka could operate as intended, there would have been no motivation for one of ordinary skill in the art to modify the subject matter taught in Saka with teachings from Sahota. In particular, the system of Saka makes corrections to a polishing process while that process is occurring. There is, therefore, no need to analyze the topography of a wafer after it has been polished, then make additional modifications of the type disclosed in Sahota; rather, it would appear based on the teachings of Saka that any additional modifications to the polishing process would be totally unnecessary. Further, the teachings of Saka would have led one of ordinary skill in the art to believe that there would be no reason to apply a force gradient based on analysis following polishing of a first semiconductor device structure to subsequently polished semiconductor device structures, as the system disclosed in Saka is configured to ensure that the planarity of each wafer polished thereby has been optimized.

Accordingly, it is respectfully submitted that the teachings of Saka and Sahota do not support a *prima facie* case of obviousness against any of claims 1-14, as would be required to maintain the 35 U.S.C. § 103(a) rejections of these claims.

Nagahara in View of Sahota

Claims 1-14 are rejected under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly unpatentable over the subject matter taught in U.S. Patent 6,351,397 to Nagahara et al. (hereinafter "Nagahara"), in view of teachings from U.S. Patent 5,665,199 to Sahota et al. (hereinafter "Sahota").

The teachings of Nagahara relate to a wafer carrier assembly 204 for use with a polishing apparatus. The wafer carrier assembly 204 includes a wafer carrier 206, which is configured to receive a backside 217 of a wafer 212. Col. 5, lines 29-31; FIG. 2a. A plurality of air lines 236a, 236b, 236c establish communication between air sources 234a, 234b, 234c and the wafer carrier 206. Col. 5, lines 45-50; FIG. 2a. A negative pressure may be applied to a central region of the backside 217 of the wafer 212 by one air line 236a to hold the wafer 212 in place within the wafer carrier 206. Col. 5, line 58, to col. 6, line 20 (*see* col. 6, lines 4 and 5, specifically); FIG. 2a. Other air lines 236b, 236c may be used to apply positive pressure to different locations on the backside 217 of the wafer 212. Col. 5, line 58, to col. 6, line 20; FIG. 2a. The application of different amounts of air pressure to different locations on the backside 217 of the wafer 212 distorts the wafer 212 in a desired manner. *See, e.g.,* col. 5, line 65, to col. 6, line 2.

It does not appear that the wafer carrier 206 is configured to isolate pressures that are communicated thereto and applied to the backside 217 of the wafer 212, nor does Nagahara teach or suggest that such isolation may occur. Thus, it appears that any pressures that are applied to the backside 217 of a wafer 212 would be evenly distributed, or at least distributed as gradients, rather than as discrete amounts of pressure.

The teachings of Sahota are summarized above.

It is respectfully submitted that there are a number of reasons that the teachings of Nagahara and Sahota do not support a *prima facie* case of obviousness against any of claims 1-14.

First, it is respectfully submitted that, without the benefit of hindsight provided by the claims of the above-referenced application, one or ordinary skill in the art wouldn't have been motivated to combine teachings from Nagahara and Sahota in the asserted manner. Specifically, it is respectfully submitted that Sahota, which teaches analysis of the topography of a semiconductor device structure to develop a polishing process that improves planarity of a material layer, discloses that tailoring a duration of polishing is sufficient for performing the desired task. Thus, use of the complex device of Nagahara in combination with the analysis technique of Sahota would only serve to complicate the polishing process of Sahota.

As one of ordinary skill in the art wouldn't have been motivated to combine teachings from Nagahara and Sahota in the asserted manner, do not support a *prima facie* case of obviousness against any of claims 1-14, as would be required to maintain the 35 U.S.C. § 103(a) rejections of claims 1-14.

Second, it is respectfully submitted that Nagahara and Sahota do not, together or separately, teach or suggest each and every element of any of claims 1-14.

Independent claim 1 is directed to a method that includes polishing a first semiconductor device structure and analyzing a topography of the first semiconductor device structure. A force gradient is generated based on the topography analysis. The force gradient includes a plurality of immediately adjacent, distinctly different amounts of pressure. The force gradient is then applied to the backside of at least one second semiconductor device structure, which is then polished.

It is respectfully submitted that neither Nagahara nor Sahota teaches or suggests generating a force gradient that includes a plurality of immediately adjacent, distinctly different amounts of pressure. Rather, Nagahara's teachings are limited to generating a gradient in which different air pressures are applied to from different locations to an open area (*i.e.*, the interior of the wafer carrier 206), which would result in mixing and, thus, the application pressure that, at one location on the backside 217 of a wafer 212, is largely indistinct from the amount of pressure applied to an immediately adjacent location on the backside 217 of the wafer 212. Sahota lacks any teaching or suggestion that any type of force gradient may be applied.

As Nagahara and Sahota do not teach or suggest each and every element of independent claim 1, the teachings of these references cannot be relied upon to establish a *prima facie* case of

obviousness against independent claim 1. As such, the subject matter to which independent claim 1 is directed is allowable over the subject matter taught in Nagahara and Sahota, taken either separately or together.

Claims 2-7 are each allowable, among other reasons, for depending directly or indirectly from independent claim 1, which is allowable.

The method of independent claim 8 also includes polishing at least one layer of a first semiconductor device structure and analyzing a topography of the active surface of the first semiconductor device structure. Distinctly increased amounts of pressure are then selectively applied to at least two locations on the backside of at least one second semiconductor device structure, relative to pressure applied to immediately adjacent areas, with the at least two locations corresponding to raised areas on an active surface of the first semiconductor device structure. The active surface of the at least one second semiconductor device structure is polished as the pressure is applied to the backside thereof.

Nagahara and Sahota both lack any teaching or suggestion of selectively applying distinctly increased amounts of pressure, relative to immediately adjacent areas of a semiconductor device structure, to at least two locations on a backside of the semiconductor device structure. Again, Nagahara teaches that air pressure may be applied to a wafer carrier 206, but lacks any teaching or suggestion that the applied air pressure is confined. As such, it would be spread out, resulting in the application of pressure at one location that is not distinctly increased relative to pressure applied at immediately adjacent locations. Sahoto also lacks any teaching or suggestion that different amounts of pressure may be applied to different locations of a semiconductor device structure.

Since Nagahara and Sahota do not teach or suggest each and every element of independent claim 8, it is respectfully submitted that the teachings of these references do not support a *prima facie* case of obviousness against independent claim 8. It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 8 is allowable over the subject matter taught in Nagahara and Sahota.

Korovin in View of Sahota

Claims 1-14 have also been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is purportedly unpatentable over the teachings of U.S. Patent 6,390,905 to Korovin et al. (hereinafter "Korovin"), in view of teachings from Sahota.

The apparatus of Korovin includes a web diaphragm 100 with a plurality of ribs 101-104. FIG. 1; col. 5, lines 54-56. In the embodiment of the apparatus shown in FIG. 1, each rib 101-104 includes a bottom edge that is configured to contact a backside of a semiconductor wafer 150. Col. 7, lines 20-24. The ribs 101-104 act as the barriers between adjacent web plenums 111-114. Col. 6, lines 10-14. Each web plenum 111-114 is configured to receive and contain pressurized fluid, which exerts pressure upon an area on the backside of the wafer 150. Col. 6, lines 53-56. Different amounts of pressure may be applied to areas of the backside that communicate with different web plenums 111-114.

The relevant teachings of Sahota are summarized above.

It is respectfully submitted that one of ordinary skill in the art wouldn't have been motivated to combine teachings from Korovin with teachings from Sahota. Specifically, it is respectfully submitted that Sahota, which teaches analysis of the topography of a semiconductor device structure to develop a polishing process that improves planarity of a material layer, discloses that tailoring a duration of polishing is sufficient for performing the desired task. Thus, use of the complex device of Korovin in combination with the analysis technique of Sahota would only serve to complicate the polishing process of Sahota. Due to this apparently unnecessary complication, it appears that the asserted combination was based solely upon impermissible hindsight.

CONCLUSION

It is respectfully submitted that each of claims 1-14 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

Brick G. Power
Registration No. 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: December 6, 2006
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